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EXAMINER	
BUEHL, BRETT J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/974,924	MAYER, ALBRECHT	
	Examiner	Art Unit	
	Brett J Buehl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/20/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-17 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment as received on 12/23/04.

Maintained Rejections

3. Applicant has failed to overcome the 35 U.S.C. 102 and 103 rejections set forth in the previous Office Action for claims 1-10. Therefore, these rejections are respectfully maintained by the examiner and copied below for applicant's convenience.

4. The examiner notes that claims 11-17, added with the current amendment, contain all the limitations of the original claims. Since the claims use "comprising" language, they are also rejected under the maintained claim rejections for claims 1-10.

Maintained Claim Rejections – 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Brooks, U.S. Patent No. 5,678,003.

7. Regarding claim 1, Brooks has taught a programmable unit, comprising:

a. At least one program operation unit for running a program (*112 of Figure 2. It is inherent that the CPU has an execution unit, i.e. "program operation unit", that executes the instructions. The IFU unit dispatches instructions to and retires instructions from the execution unit [col. 5, lines 14-17].*).

b. A stopping device (*TIU, 104, and IFU, 106, of Figure 2*) connected to said program operation unit (*Col. 5, lines 14-17. The IFU dispatches instructions, which would inherently be to an execution unit, i.e. program operation unit.*), said stopping device stopping the running of the program by said program operation unit (*col. 5, lines 34-40. When the TIU, 104, of a CPU receives a "soft_stop_debug" instruction from the scan interface tool, the TIU asserts the "soft_stop_debug" signal, 115, of the IFU, indicating a breakpoint. Then, when the break point is detected the execution of the detecting processor is stopped by allowing the IFU to finish execution of the current instructions, i.e. retires the instructions, and it is inherent that it would not dispatch further instructions. The IFU then asserts the "idle" signal to the TIU, indicating that the processor has stopped execution. Therefore, the TIU and IFU stop the operation of the processor.*), said stopping device being located on the same chip as said program operation unit (*Figure 2. The IFU and TIU are located on the processor chip.*); and

c. Other components connected to said stopping device (Other CPUs [102], *21', 23' of Figure 3, and Bus Arbiter [not shown – col. 6, lines 23-29]*), said stopping device also causing said other components to be stopped, in addition to stopping said program operation unit with which said stopping device is associated (*After the processor asserts the stop pin, 112, the other processors stop program running. Each processor then asserts a stop_req, which is detected by the interface tool. When all of the processors have asserted a stop_req bit, the interface tool issues a halt instruction to the bus arbiter, stopping all bus activity. Therefore, the stopping device associated with the processor that encountered the address breakpoint first causes the other components to be stopped by asserting a stop pin, which causes the other CPUs and the bus arbiter to stop. Since it was the stopping device that caused the chain reaction, it is responsible for stopping the system.*).

8. Given the similarities between the claims, the arguments as stated for claim 1 are also applicable to claim 11.

9. Regarding claim 2, Brooks has taught the programmable unit according to claim 1, wherein said other components include at least one further program operation unit (*Figure 3. There are 3 CPUs shown. One is the program operation unit, the other two are further program operation units.*) and said stopping device able to stop said further program operation unit which is not associated with said stopping device (*See claim 1.*).

10. Regarding claim 3, Brooks has taught the programmable unit of claim 2, wherein said other components which can be stopped by said stopping device include units which are connected to and cooperate with said program operation unit and said further program operation

unit (*21', 23' of Figure 3, and Bus Arbiter [not shown – col. 6, lines 23-29]. Tthe stopping device associated with the program operation unit is able to stop these other components, therefore these other components cooperate with the program operation unit.*)

11. Regarding claim 4, Brooks has taught the programmable unit of claim 3, wherein said units are stopped by said stopping device later in time than said program operation unit and said further program operation unit (*Figure 4. The CPUs stop first. Then, when all of the CPUs have stopped, the other units are stopped.*).

12. Given the similarities between the claims, the arguments as stated for claim 4 are also applicable to claim 12.

13. Regarding claim 5, Brooks has taught the programmable unit of claim 4, including at least one bus connected between said other components (*25 of Figure 1, Unlabeled in Figure 3*).

14. Given the similarities between the claims, the arguments as stated for claim 5 are also applicable to claim 13.

15. Regarding claim 6, Brooks has taught the programmable unit of claim 5, including bus interfaces and each of said bus interfaces is connected to one of said program operation unit and said further program running unit and to said bus, said program operation unit and said further program operation unit function as bus masters, said units are stopped only when said bus masters and said bus interfaces have no more data to output and/or are no longer waiting for already requested data or data that is still to be requested. (*Brooks discloses a system with stopping capabilities in response to "an instruction address breakpoint, data address breakpoint, single instruction step, specific JTAG instruction, or the occurrence of any particular event" [col. 6, lines 35-40]. An instruction or data address breakpoint can indicate*

the end of a program, in which case there would be no more data to output or request. The system includes several CPUs, which inherently act as bus masters since they operate independently of each other and must get data from the memory [meaning they must take control of the bus to get data]. The components in Brooks inherently contain interface logic that allows them to interact with one another through the bus and with the bus arbiter.)

16. Given the similarities between the claims, the arguments as stated for claim 6 are also applicable to claim14.

17. Regarding claim 8, Brooks has taught the programmable unit of claim 1, wherein after a stopped state of components of the programmable unit which have been stopped is cancelled, said units recommence operation before said program operation unit and said further program operation unit recommence operation. (*After the CPUs and Bus Arbiter have been stopped, the functional clocks are stopped, meaning the system has been stopped by the stopping device. After the halt is cancelled, it is inherent that the clocks would first be started [restarting the I/O and Memory], then the bus arbiter [i.e. the system is restarted in the reverse order in which it stopped]. If the CPUs were started before the bus arbiter, they could attempt to access Memory though the bus arbiter, causing an unnecessary fault. Therefore, the system would be started in reverse order.*).

18. Given the similarities between the claims, the arguments as stated for claim 8 are also applicable to claim 16.

19. Regarding claim 9, Brooks has taught the programmable unit of claim 6, wherein said units function as bus slaves and after a stopped state of components which have been stopped is cancelled, only said bus slaves recommencing operation, and said bus masters recommencing

operation only after said bus slaves have recommenced operation (*See rejection for Claim 8. The I/O, Memory and Bus Arbiter are the slaves, since they operate to accommodate the bus masters [i.e. CPUs]*).

20. Regarding claim 10, Brooks has taught the programmable unit of claim 1, wherein said stopping device is an on-chip debug support module (*IFU and TIU of Figure 3. These components comprise the stopping device and are responsible for stopping the system during debug mode. Since it is on the processor chip, it is an "on-chip debug support module".*).

21. Given the similarities between the claims, the arguments as stated for claim 10 are also applicable to claim 17.

Maintained Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks, and further in view of Hennessy.

24. Regarding claim 7, Brooks discloses the invention substantially as claimed. Brooks, however, does not disclose the bus including first and second parts, with a bus bridge connecting the two bus parts.

25. While Brooks has taught a single bus comprising all of the limitations of claim 7, Brooks has not explicitly taught the bus comprising a second portion. However, the inclusion of a

second bus portion with no reference in the claim as to how it is configured in relation to the first portion of the bus provides no new or unexpected result over the prior art of record. Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to duplicate the bus, creating a second bus comprising all of the limitations of the first bus of Brooks (see In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

26. Alternatively, Hennessy has taught that it was well known in the art at the time of the invention to include in a computer system several buses, which inherently have a bus bridge to connect the buses, that allow for additional connectivity to different types of peripheral devices, which "offers the advantage that the processor-memory bus [first bus] can be made much faster than a backplane or I/O bus [second bus] and that the I/O system can be expanded by plugging many I/O controllers or buses into the backplane bus, which will not affect the speed of the processor-memory bus" (Page 658 of Hennessy). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Brooks to contain more than one bus connected through a bus bridge so a wider range of peripheral devices can be coupled to the system resulting a wider range of peripheral devices being able to be coupled to the system without sacrificing the speed of the faster bus.

27. Given the similarities between the claims, the arguments as stated for claim 7 are also applicable to claim 15.

Response to Remarks

28. Applicant's arguments filed on 23 December 2004, have been fully considered but they are not persuasive.

29. Applicant argues the novelty/rejection of claim 1 and 10, on pages 10-14, and claim 11 on pages 14-18 of the remarks, in substance that:

"the Brooks reference does not teach that the device responsible for stopping the processor is located on-chip with the processor."

"the element responsible for stopping the processor in Brooks, is not the TIU 104, but the externally connected scan interface tool 14."

"Applicant believes that the Brooks reference fails to teach or suggest that peripherals are connected to the scan interface tool 14 of that reference"

"the Brooks reference fails to teach or suggest, among other limitations of Applicant's claims, 'peripherals connected to said stopping device, said stopping device also causing said peripherals to be stopped."

30. These arguments are not found persuasive for the following reasons:

31. The applicant argues that the scan interface tool, 14, is responsible for stopping the processor, not the TIU, 104. The examiner notes that the scan interface tool issues a "soft_debug_stop" instruction to the processors to indicate that they are in debug mode. The TIU and TFU, however, are the devices responsible for the actual stopping of the processor (See arguments for claim 1). Once the breakpoint is detected, the processor that detected it signals for the other processors to stop via a stop pin. This pin is directly connected to the other processors. When the other processors detect the signal, the corresponding IFU allows the current instructions to finish (same as on the processor detecting the breakpoint) and stops the processor. Each processor then sets a bit in its JTAG register, indicating it has stopped. The scan interface tool then issues a halt instruction to the bus arbiter when all of the processors indicate that they

have stopped. It is noted by the examiner that claim 1 states "said stopping device also causing said other components to be stopped." The stopping device in Brooks, IFU and TIU, cause the other CPUs to stop at the same time as the detecting CPU. In addition, the stopping device also causes the other components, i.e. the bus arbiter and memory, to be stopped by setting its stop_req bit and signaling to the other CPUs to stop, thereby setting their stop_req bits. Therefore, the stopping device of Brooks stops the other components. The stopping may be done with the aid of other components, but it is the stopping device that ultimately causes the system to stop.

32. The applicant argues that the stopping device in Brooks is not located on the same chip. Referring to the arguments above, the examiner notes that the IFU and TIU are located on the processor chip. Therefore, the stopping device is located on chip.

33. The applicant argues that Brooks does not teach peripheral devices connected to the stopping device. However, Brooks has taught an I/O unit, memory and a bus arbiter. These components are considered peripheral devices. Since the stopping unit is part of the CPU, which is connected to the peripheral devices through the system bus, the stopping unit is connected to the peripheral devices. As for the stopping device being able to cause the peripheral devices to stop, see the arguments stated above.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Inquiries concerning this communication or earlier communications from the examiner should be directed to Brett J. Buehl who can be reached at (703) 305-4663, or <brett.buehl@uspto.gov>. Starting on October 13, 2004, Brett Buehl can be reached at (571) 272-4161. The examiner can normally be reached between the hours 8:30am – 6:00pm (EST), Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan, can be reached at (703) 305-9712. Starting on October 13, 2004, Eddie Chan can be reached at (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

36. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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